2nd Sem D.E

USN | | | | | | | | | | |

12EC009

M.Tech. Degree Examination, June/July 2014
Advances in VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Describe the operation of NMOS and PMOS transistors as switches and their short comings. **(04 Marks)**

b. Explain the main advantage and disadvantage of using a CMOS implementation for transmission gates instead of pure NMOS or pure PMOS implementation. **(04 Marks)**

c. Explain with suitable circuit diagram the implementation of a simple BiCMOS inverter. Also, explain the two main issues with this simple BiCMOS inverter implementation. **(12 Marks)**

2 a. With suitable diagrams, explain the structure and IV characteristics of a MESFET corresponding to below pinch-off and at pinch-off. **(08 Marks)**

b. With a neat sketch, describe the structure of a MODFET and explain the band diagrams associated with this structure. **(10 Marks)**

c. Explain how a MODFET is suitable for high frequency applications. **(02 Marks)**

3 a. Explain with a figure the capacitance variation with voltage and frequency for a P-type MIS structure. **(06 Marks)**

b. Draw the small signal equivalent circuit model for a MOSFET operating at high frequency and derive the expression for cut-off frequency for this device. What parameters have maximum control of the cut-off frequency of this device? **(10 Marks)**

c. Calculate the cut-off frequency of a n-channel MOSFET with channel length = 1.5μ, surface mobility = 750 cm^2/vs, threshold voltage V_T = 1V and V_G = 3V. **(04 Marks)**

4 a. Derive an expression to show the relationship between the drain currents for a short channel P-type MOSFET and the drain current for a long channel equivalent device. Assume the expression for the drain current for long channel devices. **(08 Marks)**

b. What is constant electric field scaling? What is scaled? **(02 Marks)**

c. Show that in constant electric filed scaling, the threshold voltage and drain current scale linearly with dimensions and voltage. **(08 Marks)**

d. What are Moore's 1st and 2nd law? **(02 Marks)**

5 a. Give two major advantages of designing with pass transistor logic (PTL). **(02 Marks)**

b. Explain with figures, the three important rules to be followed in designing PTL (assume n-MOS). **(09 Marks)**

c. For a NMOS PTL based 2 input NAND gate, give the modified truth table, the resulting K-MAP and one implementation of the function. **(08 Marks)**

d. Show how the danger of tristated outputs is avoided in the above implementation. **(01 Marks)**

6 a. Draw the CMOS implementation of the AND-OR-INVERT (AOI) logic function as a transistor circuit diagram. $Y = \overline{A.B + B.E}$. **(05 Marks)**

b. Draw the stick diagram corresponding to the above AOI implementation (clearly indicate the signals and layers). **(05 Marks)**

c. Describe the function of a 4-input tally circuit using an appropriate block diagram make suitable assumptions. **(05 Marks)**

d. Implement the above 4-input tally function using a ROM (make suitable assumptions and show content of the ROM). **(05 Marks)**

7 a. It is required to evaluate various implementation methodologies for a new project. The target implementations are FPGA, gate array, standard cell and full custom. Rate (4 is highest and 1 is lowest) these methodologies for i) Engineering effort; ii) Engineering cost; iii) Device cost; iv) Performance. Show the ratings as a suitable table. **(08 Marks)**

b. With a suitable example, explain the below terms: i) Hierarchy; ii) Regularity; iii) Modularity; iv) Locality. **(12 Marks)**

8 Write short notes on:

a. Advantages of SOI FETs. **(10 Marks)**

b. Advantages and disadvantages of BiCMOS technology. **(10 Marks)**

* * * * *